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ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/992,076	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in the office action dated 10 August 2006. Applicants' response of 14 November 2006 has amended claims 1, 7, 8, 15, and 19. Claims 1-20 have been submitted for reconsideration.

Claims 1-20 are rejected.

Drawings

The previous objections to the drawings are withdrawn in response to the 14 November 2006 submission.

Claim Rejections - 35 USC § 101

The previous rejection of claims 7, 8, and 19 under 35 U.S.C. § 101 has been withdrawn in response to the amendments to these claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 7, 8, and 19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the

claimed invention. The application as filed does not describe displaying memory contents or states of CPUs for comparison for consistency, as recited by claims 7, 8, and 19.

Claim Rejections - 35 USC § 112

The previous rejection of claims 7, 8, and 19 under 35 U.S.C. § 112, second paragraph, has been withdrawn in response to the amendments to these claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7, 8, and 19 are rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the "display" components upon which contents of a first and second memory are displayed for comparison.

Response to Arguments – 35 U.S.C. § 103

In response to the previous rejections of claims 1-2, 5-11, 13-16, and 18-20 under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Grunert and further in view of Jackson, Applicants argue primarily that:

> Johnson fails to teach or suggest that a microcontroller is installed on a test circuit, as claimed.

The Examiner respectfully traverses this argument as follows.

Johnson has not been cited as teaching microcontrollers. Grunert has been applied as teaching microcontrollers. Inasmuch as Applicants are attempting to distinguish the term "test

circuit" from the prior art, the entire circuit arrangement disclosed by Johnson is for the purposes of testing (column 4, line 59 – column 5, line 11, for example), and therefore a "test circuit".

Applicants further argue that:

> The rejection fails to show an ICE coupled to a computer system, as claimed. Accordingly, Johnson fails to teach or suggest an ICE coupled to a computer system, as claimed.

The Examiner respectfully traverses this argument as follows.

As set forth in the previous rejection, Johnson teaches an ICE (in circuit emulator) including a second memory and a second CPU coupled to a computer system separate from said ICE [FIG. 1, references 14, 15, and 18; *"As will be seen hereinafter, the system 10 is configured to permit the in circuit emulator 18 to verify the execution by the processors 12 and 14 of the execution instructions to be executed by the processors."* (column 3, lines 53-56)]. Applicants' attention is respectfully drawn to FIG. 1, where reference 14 depicts a "slave **processor**," reference 15 depicts **"cache" memory** of the slave processor, and reference 18 depicts an "**in circuit emulator**." Other components of the disclosed invention, represented as lines and arrows, show the **connection** between the references 14, 15, and 18.

Applicants have not set forth and the Examiner cannot find an explicit and deliberate definition for the term "computer system" that distinguishes Applicants' use of the term from the normal and ordinary meaning.

Applicants further argue that:

> As Applicant understands, the rejection seems to suggest that since Johnson does not disclose that the bus 34 (see Johnson, Figure 1 element 34) prevents data transmission, it must therefore enable data transmission between the test circuit and the computer system, as claimed. The Applicant respectfully reminds the Examiner that the omission of a teaching in a reference does not necessarily teach the opposite

> of that teaching, as seems to be suggested by the rejection. Moreover, the Applicant respectfully reminds the Examiner that to establish a *prima facie* case of obviousness the prior art (or references when combined) must teach or suggest all the claim limitations (citations omitted). Therefore, it is improper to rely on Johnson failing to disclose that the bus 34 prevents data transmission to show that it somehow enables data transmission between the test circuit and the computer system, as claimed by the present embodiment. Accordingly, Johnson fails to explicitly teach or suggest an interface enables data transmission between the test circuit and the computer system as claimed.

The Examiner respectfully traverses this argument as follows.

Applicants' attention is respectfully drawn to the claim language, which states (emphasis added):

> An interface for coupling the test circuit and the ICE ***enabling*** data transmission between the test circuit and the computer system...

Applicants' claim language does not positively recite the transfer of data. The plain meaning of the claim language is that the interface ***enables*** the transfer of data. The Johnson references teaches precisely what Applicants have claimed, that is, an interface for coupling the test circuit and the ICE ***enabling*** data transmission between the test circuit and the computer system.

In the event that Applicants seek patent protection for, *inter alia*, transferring data, the Examiner respectfully suggests claim language that positively recites that feature.

Further, Microsoft Computer Dictionary, Fifth Edition provides the following definition:

> **bus *n.*** A set of hardware lines (conductors) used for data transfer among the components of a computer system.

Therefore the Examiner maintains that the bus described by Johnson ***enables*** the transfer of data between the connected components.

Applicants further argue that:

> The teaching by Grunert does not necessarily teach or suggest operating in lock step by executing the same instructions using the same clocking signals, as claimed. For example, operating as a master and a slave and having a clock synchronizing the master and slave is to clock the two microcontrollers two cycles apart.

The Examiner respectfully traverses this argument as follows.

Grunert explicitly discloses that "[t]he slave receives the same program instructions parallel to the master" (column 1, lines 48-65) and are synchronized by a single clock (column 2, lines 58-59). Therefore it appears to the Examiner rather plain that Grunert teaches lock step synchronization by executing the same instructions using the same clocking signals, as claimed.

There appears to be no factual support in the references of record for Applicants' argument that "having a clock synchronizing the master and slave is to clock the two microcontrollers two cycles apart." This description of the prior art reference appears to clearly contradict the ordinary meaning of "synchronizing".

Applicants further argue that:

> Jackson fails to teach or suggest a computer system separate from the ICE configured to compare a content of the first memory against a content of the second memory to verify the lock step, as claimed.

The Examiner respectfully traverses this argument as follows.

Jackson has not been cited to teach "a computer system separate from the ICE." To quote the previous rejection, "*Jackson teaches comparing contents of a first memory against a contents of a second memory to verify lock step operation.*" Applicants do not appear to contest that finding of fact. Therefore, the teachings found in Johnson, including "comparing a contents of a first memory against a contents of a second memory" do support the finding of obviousness, in combination with the other references, as explicitly set forth in the previous office action.

Applicants further argue that:

> Claim 9 recites initializing a first memory of an ICE and a second memory of a microcontroller with microcontroller test code, as claimed.

Applicants' arguments apparently suggest that the prior art does not teach initializing a computer memory with the instructions for execution. Naturally, the prior art teaches this old, well known, and necessary step to achieve any level of operability [*"To do so, the in circuit emulator includes a duplicate of the program instructions in its own memory and receives from the processor, the external memory fetch addresses, the obtained instructions and data, and execution status signals."* (Johnson, column 1, line 61 – column 2, line 5, etc.)].

These quotations will be included in the rejection for Applicants' convenience.

The concept of a "stored program" is at least as old as the well-known von Neumann computer architecture, which forms the basis for modern computer technology. For Applicants' convenience, the Examiner has provided an informative Wikipedia article regarding von Neumann architecture. That article is provided merely for its informational content and is not relied upon for any rejection under 35 U.S.C. § 103.

Applicants further argue that:

> Independent claim 9 further recites reporting an error and saving an execution history using a trace buffer if lock step execution is not verified, and continuing execution of the microcontroller test code if lock step execution is verified, as claimed.

Jackson teaches reporting an error if lock step execution is not verified [*"the error output on each chip is fed back to the data processing logic, in order to inform the logic that an error has occurred, so that an appropriate response can be taken."* (column 3, lines 16-19)].

Johnson teaches saving an execution history using a trace buffer coupled to the ICE [*"In accordance with the preferred embodiment, the internal execution parameter to be provided by the processor 14 is the address of the internal caches 13 and 15 for a non-sequential fetch to the internal caches. This, when combined with the information of when the pipeline is advanced, stalled, branching, or taking a trap, can give the in circuit emulator the instruction trace information it needs."* (column 5, line 68 – column 6, line 7)].

Johnson teaches continuing execution of the microcontroller test code [*"As can also be appreciated, the instructions stored in the external memory constitute the program for the processor."* (column 1, lines 56-60)]. A "program" is a sequence of instructions.

These quotations will be included in the rejection for Applicants' convenience.

Applicants further argue that:

> Regarding claim 6... The Applicant does not understand a master/slave configuration to necessarily have a program counter wherein lock step execution is maintained by maintaining the program counters in lock step, as claimed.

The Examiner respectfully traverses this argument as follows.

Grunert explicitly discloses that the master and slave are two identical microcontrollers (column 1, lines 48-51) which receive the same program instructions (column 1, lines 51-52) and are synchronized by a single clock (column 2, lines 58-59). It is a necessary and inherent result of this arrangement that the program counters of the microcontrollers are maintained in lock step.

Applicants further argue that:

> Regarding Claims 7, 8, and 19... The Applicant respectfully submits that Jackson fails to teach or suggest displaying a content of memory, or displaying the state of CPUs capable of comparison for consistency when execution of the microcontroller is halted, as claimed.

The Examiner respectfully traverses this argument as follows.

These limitations have been rejected under 35 U.S.C. § 112, first and second paragraphs, for inadequate written description and omitting essential elements. According to the teachings of the specification, these limitations appear to mean "issuing a signal indicating a 'lock-step error'" (specification, page 5, lines 6-12). There appears to be no teaching in the specification of a display device such as a computer monitor, and no teaching of a graphical display of the contents of a first and second memory for the purposes of comparison.

Grunert teaches lock step synchronization by executing the same instructions using the same clocking signals (column 1, lines 48-65; column 2, lines 58-59).

Jackson teaches comparing contents of a first memory against a contents of a second memory to verify lock step operation (column 1, lines 46-66; column 1, line 67 – column 2, line 2; column 1, lines 11-21).

Jackson teaches issuing an error signal [*"If the outputs of the two chips do not compare, an error signal is generated in a manner similar to that described with respect to FIG. 1"* (column 4, lines 8-18)].

Therefore, the prior art as applied to the claims below renders obvious the limitations of claims 7, 8, and 19.

Applicants further argue that:

> Regarding claim 14... The Applicant respectfully submits that Jackson fails to teach or suggest halting the execution when a breakpoint is encountered, and verifying lock step while execution is halted, as claimed.

The Examiner respectfully traverses this argument as follows.

Microsoft Computer Dictionary, Fifth Edition provides the following definition:

breakpoint ***n.*** A location in a program at which execution is halted so that a programmer can examine the program's status, the contents of variables, and so on. A breakpoint is set and used within a debugger and is usually implemented by inserting at that point some kind of jump, call, or trap instruction that transfers control to the debugger.

The Johnson reference is directed to debugging [*"During program development, it is advantageous to verify the correctness of the program instructions stored in the external memory to be executed by the processor. Such program verification, referred to as debugging, can employ an in circuit emulator. In circuit emulators are well known in the art and are used to track the execution of a processor."* (column 1, lines 61-67)].

The Grunert reference expressly teaches breakpoints [*"The internal state of the master 2 can be traced by setting breakpoints."* (column 5, lines 9-25)].

The Examiner respectfully submits that a person of ordinary skill in the art, confronted with the prior art of record, would find "halting execution when a breakpoint is encountered" to be obvious within the meaning of 35 U.S.C. § 103.

Further, the Jackson reference teaches verifying lockstep continuously. This teaching certainly encompasses "verifying lock step while execution is halted" because a breakpoint was encountered.

Applicants have also argued for the patentability of dependent claims by virtue of their dependence. Those arguments have been addressed above.

Applicants' arguments have been fully considered but have been found unpersuasive.

In the interest of compact prosecution, Applicants may find it expeditious to hold an interview with the Examiner to discuss the technical merits of the prior art. In many circumstances, technical concepts relevant to the prior art can be quickly and effectively addressed via telephone interview, thereby advancing prosecution.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

3. Claims 1-2, 5-11, 13-16, and 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,357,626 to Johnson et al. (Johnson) in view of US Patent No. 6,366,878 to Grunert and further in view of US Patent No. 4,176,258 to Jackson.

Regarding claims 1, 9, 11, and 15, Johnson teaches a system for debugging code [*"The present invention is generally directed to an arrangement for verifying, with an in circuit emulator, the instructions to be executed by a processor of a processing system."* (column 1, lines 10-13)] comprising:

A processor installed on a test circuit, wherein the processor includes a first memory and a first CPU [FIG. 1, references 12 and 13; *"As thus far described, the microprocessors 12 and 14 are configured for executing instructions stored externally in the external memory 16."* (column 5, lines 12-14); *"However, as will be noted in FIG. 1, each of the processors 12 and 14 includes an internal instruction cache 13 and 15 respectively."* (column 5, lines 44-49)];

An ICE (in circuit emulator) including a second memory and a second CPU coupled to a computer system separate from said ICE [FIG. 1, references 14, 15, and 18; *"As will be seen hereinafter, the system 10 is configured to permit the in circuit emulator 18 to verify the execution by the processors 12 and 14 of the execution instructions to be executed by the processors."* (column 3, lines 53-56)];

Wherein the ICE emulates the processor [*"To enable the second processor 14 to duplicate the executions of the first processor 12, the second processor 14 includes a multiple-bit instruction/data input 36 which is coupled to the external instruction/data bus 34."* (column 4, lines 31-34)];

The processor and the ICE run the processor code in lock step by executing the same instructions using the same clocking signals [*"To control system timing, the first processor 12 includes a clock input 40 and the second processor 14 includes a clock input 42. The clock inputs 40 and 42 are coupled together by an INCLOCK line 44 which is adapted to be coupled to an external clock source (not shown)."* (column 4, lines 35-40)]; and

An interface for coupling the test circuit and the ICE [FIG. 1, reference 34, etc.; *"To enable the second processor 14 to duplicate the executions of the first processor 12, the second processor 14 includes a multiple-bit instruction/data input 36 which is coupled to the external instruction/data bus 34."* (column 4, lines 31-34)], that interface does not prevent transmission between the test circuit and the computer system.

Johnson does not expressly teach that the processors are microcontrollers.

Grunert teaches the use of microcontrollers (abstract). In particular, Grunert teaches two microcontrollers operating in lock step, wherein the second microcontroller emulates the first microcontroller [*"The overall circuit arrangement 1, shown in FIG. 1, for in-circuit emulation includes two microcontrollers 2, 3... The microcontroller 2 is operated as master, the microcontroller 3 as slave"* (column 4, lines 26-39); *"The emulation operation is controlled by*

means of a service computer connected to the circuit arrangement 1." (column 5, lines 10-25); *"In accordance with another feature of the invention, a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)].

Johnson and Grunert are analogous art because they are from the same field of endeavor of in-circuit emulation.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Johnson system by replacing the processors 12 and 14 with microcontrollers as taught by Grunert.

The motivation for doing so would have been to verify the operating program of a production microcontroller. Grunert teaches how to easily access this operating program [*"In particular, there is a need to provide a possibility of access to the operating program of the microcontroller, which in normal operation is stored in an ROM memory which is not directly accessible from outside."* (column 1, lines 9-22)].

Therefore, it would have been obvious to combine Grunert with Johnson to obtain the invention.

Johnson in view of Grunert does not expressly teach comparing contents of a first memory against contents of the second memory to verify the lock step operation.

Jackson teaches comparing contents of a first memory against a contents of a second memory to verify lock step operation [*"The inputs of the chips are externally wired in parallel, and since the chips receive the same input data, they should each generate the same output at*

any instant of time." (column 1, lines 46-66); *"The invention has the advantage that when operating properly, both chips should be in exactly the same state throughout all time and therefore the outputs should agree."* (column 1, line 67 – column 2, line 2); and more generally, *"Redundant checking systems are well known in prior art. For example, in the past, two identical logic circuits have been wired in parallel, the same input information being supplied to each, with the output of each circuit being compared in a comparison checking circuit for equality. For example, two identical computers have been operated side-by-side with the same problem being supplied to each. A comparison of the results from each computer at some point in the computation indicates whether one of the computers has malfunctioned."* (column 1, lines 11-21)].

Jackson and Johnson in view of Grunert are analogous art because both are directed to verifying the operation of computer hardware or software.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to compare the outputs of the microcontroller processors (*i.e. register contents or stored memory contents*) to verify lock step operation.

The motivation for doing so would have been to determine whether one of the microcontrollers had malfunctioned, as expressly taught by Jackson and described by Jackson as well known in the art (Jackson, column 1, lines 11-21).

Therefore, it would have been obvious to combine Jackson with Johnson in view of Grunert to obtain the invention as specified in claim 1.

Further regarding the language of claim 9, Jackson teaches reporting an error if lock step execution is not verified [*"the error output on each chip is fed back to the data processing logic, in order to inform the logic that an error has occurred, so that an appropriate response can be taken."* (column 3, lines 16-19)].

Johnson teaches saving an execution history using a trace buffer coupled to the ICE [*"In accordance with the preferred embodiment, the internal execution parameter to be provided by the processor 14 is the address of the internal caches 13 and 15 for a non-sequential fetch to the internal caches. This, when combined with the information of when the pipeline is advanced, stalled, branching, or taking a trap, can give the in circuit emulator the instruction trace information it needs."* (column 5, line 68 – column 6, line 7)].

Johnson teaches continuing execution of the microcontroller test code [*"As can also be appreciated, the instructions stored in the external memory constitute the program for the processor."* (column 1, lines 56-60)]. A "program" is a sequence of instructions.

Regarding claims 2, and 16, Grunert teaches that the microcontroller is installed on a pod [*"It is expedient for the microcontrollers 2, 3 to be arranged right next to one another on the printed circuit board, in order to be able to achieve as high an operating frequency as possible. A clock system 5 ensures good synchronization between master 2 and slave 3."* (column 5, lines 5-9)].

Regarding claims 5 and 18, Grunert teaches that the microcontrollers have a plurality of registers [*"The corresponding ports P5', P6', are therefore free in the slave 3, with the result*

that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, ***register contents****, etc. or for controlling the program execution."* (column 5, lines 10-25)].

Regarding claim 6, Johnson teaches that the first CPU and second CPU each have a program counter which are maintained in lock step [*"To that end, and as will be more fully described hereinafter, the first processor 12 and second processor 14 are coupled together in a master/slave configuration to permit the second processor 14, which is the slave processor, to duplicate the instructions performed by the first processor 12, which is the master processor."* (column 3, lines 57-62)].

Regarding claims 7, 8, and 19, Jackson teaches that a content of said first memory and a content of said second memory (and a state of a first CPU and a state of a second CPU) are "displayed for comparison" for consistency when execution of the microcontroller is halted [*"the error output on each chip is fed back to the data processing logic, in order to inform the logic that an error has occurred, so that an appropriate response can be taken."* (column 3, lines 16-19); *"If the outputs of the two chips do not compare, an error signal is generated in a manner similar to that described with respect to FIG. 1"* (column 4, lines 8-18)]. The application appears to define "displaying for comparison" as "generating a signal." See Response to Arguments above, and specification page 5, lines 6-12.

There appears to be no suggestion in any of the cited references that a person would be unable to do so when the execution of the code is halted. That is, Jackson teaches "comparing" at all times, including when the execution of code is halted.

The Johnson reference is directed to debugging [*"During program development, it is advantageous to verify the correctness of the program instructions stored in the external memory to be executed by the processor. Such program verification, referred to as debugging, can employ an in circuit emulator. In circuit emulators are well known in the art and are used to track the execution of a processor."* (column 1, lines 61-67)].

The Grunert reference expressly teaches breakpoints [*"The internal state of the master 2 can be traced by setting breakpoints."* (column 5, lines 9-25)].

Further regarding claim 14, the Johnson reference is directed to debugging [*"During program development, it is advantageous to verify the correctness of the program instructions stored in the external memory to be executed by the processor. Such program verification, referred to as debugging, can employ an in circuit emulator. In circuit emulators are well known in the art and are used to track the execution of a processor."* (column 1, lines 61-67)].

The Grunert reference expressly teaches breakpoints [*"The internal state of the master 2 can be traced by setting breakpoints."* (column 5, lines 9-25)].

Further, the Jackson reference teaches verifying lockstep continuously (entire document, FIG. 1 depicting hardwired circuitry). This teaching certainly encompasses "verifying lock step while execution is halted" because a breakpoint was encountered.

When forming the combination of claim 9, and in combination with these teachings in the prior art, it would have been obvious to a person of ordinary skill in the art to halt the execution of the microcontroller test code when a breakpoint is encountered, and verifying lock step execution by comparing content of the first memory and content of the second memory while the execution is halted.

Regarding claim 10, Johnson teaches locating an error within the test code by tracing the execution history using a trace buffer [*"As thus far described, the system 10 is capable of providing the in circuit emulator 18 with sufficient information to track the executions of the processors 12 and 14 of external instructions stored in the external memory 16."* (column 5, lines 40-44) describes "tracing" the execution history; *"This, when combined with the information of when the pipeline is advanced, stalled, branching, or taking a trap, can give the in circuit emulator the instruction trace information it needs."* (column 6, lines 4-8)].

Regarding claims 13 and 20, Grunert teaches that the microcontroller is a production microcontroller [*"When the standard commercially manufactured microcontroller is present, in-circuit emulation is also already possible. It is advantageous that all design changes carried out in the standard commercially manufactured product (for example time response of connecting ports and switching edges, live currents, etc.) are also directly available in the emulator."* (column 1, lines 59-65)].

4. Claims 3, 12, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Grunert and further in view of Jackson, as applied to claims 1, 9, and 15 above, and further in view of US Patent No. 6,173,419 to Barnett.

Regarding claims 3, 12 and 17, none of Johnson, Grunert or Jackson expressly teaches that the microcontroller is copied in an FPGA.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55).

Barnett and Johnson in view of Grunert and further in view of Jackson are analogous art because all are directed to computer hardware.

Therefore it would have been obvious to a person of ordinary skill at the time of Applicants' invention to copy a microcontroller in an FPGA of the emulator.

The motivation for doing so would have been to produce a reconfigurable emulator [*"The emulator is programmed into a field programmable gate array (FPGA) which will work in real time, does not need to be fabricated as an expensive ASIC, and is programmable to other configurations."* (column 5, lines 31-36)].

Therefore it would have been obvious to combine Barnett with Johnson in view of Grunert and further in view of Jackson to obtain the invention as specified in claims 3, 12, and 17.

5. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Grunert and further in view of Jackson as applied to claim 1, further in view of "State of the Art" by Stan Augarten, published 1983 (Augarten).

None of Johnson, Grunert, or Jackson expressly teaches that the first and second memories are SRAM.

Augarten discloses that SRAM has been known in the art since 1970. Augarten expressly teaches the advantages of SRAM [*"The charges in static RAMs do not leak away, freeing such chips from the need for periodic refreshing" ... "this chip was able to retain, in the space of a single core, many times the amount of information"* (third paragraph)]

Augarten and Johnson in view of Grunert and further in view of Jackson are analogous art because all are directed computer hardware.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use the well-known technology of SRAM in the microcontrollers.

The motivation would have been avoiding the need to periodically refresh the charges and to store more data in a smaller space [*"The charges in static RAMs do not leak away, freeing such chips from the need for periodic refreshing" ... "this chip was able to retain, in the space of a single core, many times the amount of information"* (third paragraph)].

Therefore, it would have been obvious to combine Augarten with Johnson in view of Grunert and further in view of Jackson to obtain the invention as specified in claim 4.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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1/26/07